IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: NEMAZIE et al.	Art Unit: 2181
Appl. No.: 10/775,521	Examiner: Lee, Chun Kaun
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For: Switching Serial Advanced Technology Attachment (SATA) to a Parallel Interface	

Amended Appeal Brief Under 37 CFR § 41.37

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Commissioner for Patents
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Sir:

In response to the Notification of Non-Compliant Appeal Brief mailed March 21, 2008, Appellants submit this amended appeal brief under 37 CFR § 41.37.

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III. STATUS OF CLAIMS

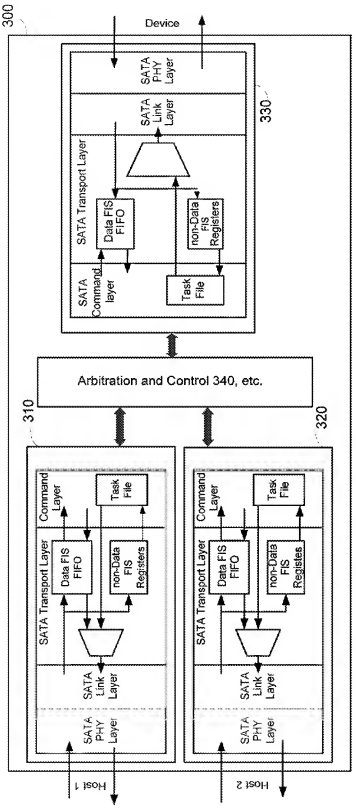
A. Pending Claims

Claim 1 has been rejected and is the subject of this appeal. Claims 2 and 3 have been canceled and are not the subjects of this appeal. Claim 4 has been rejected and is the subject of this appeal. Claim 5 has been canceled and is not the subject of this appeal. Claims 6-19 have been rejected and are the subjects of this appeal. Claim 21 has been canceled and is not the subject of this appeal. Claims 22-32 have been rejected and are the subjects of this appeal. Claims 33 and 34 have been canceled and are not the subjects of this appeal. Claims 35-43 have been rejected and are the subjects of this appeal. Of these, claims 1, 18, and 31 are independent claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed subject matter relates to enabling multiple hosts to concurrently access a single storage device using industry-standard Serial Advanced Technology Attachment (SATA) interface protocol.

By way of convenience, an exemplary embodiment of the present invention is illustrated in the figure below, which is a condensed representation of Fig. 6 from the patent application.


300
Device
SATA PHY Layer
SATA Link Layer
330
SATA Transport Layer
Data FIS FIFO
non-Data FIS Registers
SATA Command layer
Task File
Arbitration and Control 340, etc.
310
320
Command Layer
Task File
SATA Transport Layer
Data FIS FIFO
non-Data FIS Registers
SATA Link Layer
SATA PHY Layer
Host 1
Host 2

In general, the switch 300 includes SATA ports 310 and 320, which are coupled to hosts 1 and 2, respectively. The switch 300 further includes SATA port 330, which is coupled to a Device. The Device is generally a storage device. The features of the various embodiments of the present invention allow the hosts concurrent access to the Device. Concurrency, as used herein, indicates acceptance of commands, from either of two or more hosts, at any given time including when the Device (such as a storage unit) is not in an idle state.

Turning now to the claimed subject matter, claim 1 is directed towards "a switch coupled between a plurality of host units and a device for communicating therebetween." Claim 1 recites in part "comprising: a first serial advanced technology attachment (ATA) port coupled to a first host unit and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit." Claim 1 further recites "a second serial ATA port coupled to a second host unit and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit." Claim 1 further recites "a third parallel ATA port, coupled to a device, for causing access to the device, by the first or second host units." Lastly, claim 1 includes "an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state."

Thus, various embodiments of the present invention innovatively teach using a host task file in each SATA port. It is noted that the first and second task files are located before the arbitration and control circuit therefore allowing concurrent acceptance of commands from the hosts.

Figure 12 of the instant specification show how, by using reserved bits in the FIS, the FIS organization can be modified to identify the host originating the FIS, making routing of the FIS transparent to the switch.

Claim 4 further defines the switch in claim 1 "wherein said third parallel ATA port includes a device task file.

Claim 5 further defines the switch in claim 4 "wherein said first, second and third ports are level 4 ports."

Claim 6 further defines the switch as recited in claim 1. Thus, claim 6 recites "wherein said device is a storage unit."

Claim 7 still further defines where the switch in claim 1 is employed. Thus, Claim 7 recites "wherein said switch is employed in an enterprise system."

Claim 8 further defines the switch as recited in claim 1 "wherein said arbitration and control circuit causes concurrent access to the device by the first and second host units."

Claim 9 further defines the switch in claim 1 "wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units."

Claim 10 further defines the switch in claim 9. Thus, claim 10 recites "wherein the information is referred to as 'identity drive response.'"

Claim 11 further defines the switch in claim 9 wherein "the information is referred to as 'Tag.'"

Claim 12 further defines the switch in claim 1 "wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device."

Claim 13 further defines the switch as recited in claim 12. Thus, claim 13 recites "wherein the information is referred to as 'Tag.'"

Claim 14 further defines the switch in claim 13 "wherein the arbitration and control circuit include a Tag/Sactive Mapping Circuit for mapping a host tag to a device tag and inverse mapping for identifying a host."

Claim 15 further defines the switch in claim 1 "wherein either the first or the second host sends a legacy queue command queued by the device."

Claim 16 further defines the switch in claim 1 "wherein either the first or the second host sends a native queue command for execution thereof by the device."

Claim 17 further defines the switch in claim 1 "wherein the first, second and third ports are level 3 ports and a Data frame information system (FIS) first-in-first-out (FIFO) and an associated FIFO Control are coupled to the first, second and third ports and located external thereto."

Claim 18 is directed towards a switch "comprising: a first serial advanced technology attachment (ATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit." Claim 18 further recites that the switch also includes "a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit." Claim 18 still further recites "a third parallel ATA port for connection to a device." Lastly, claim 18 states that the switch includes "an arbitration and control circuit, coupled to the first, second and third ports, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state."

Claim 19 further defines the switch in claim 18 wherein "the switch is a serial ATA switch."

Claim 22 further defines the switch in claim 18 "wherein said third parallel ATA port includes a device task file."

Claim 23 further defines the switch in claim 18 "wherein said device is a storage unit."

Claim 24 further defines the switch recited in claim 18 "wherein said switch is employed in an enterprise system."

Claim 25 further defines the switch in claim 18 "wherein said arbitration circuit causes concurrent access of the device by the first and second host units."

Claim 26 further defines the switch in claim 18 "wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units."

Claim 27 further defines the switch in claim 26 "wherein the information is referred to as 'identity drive response.'"

Claim 28 further defines the switch in claim 26 "wherein the information is referred to as 'Tag.'"

Claim 29 further defines the switch in claim 18. Thus, claim 29 recites "wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device."

Claim 30 further defines the switch in claim 28 "wherein the information is referred to as 'Tag.'"

Claim 31 is directed towards a switch "that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (SATA) links." Claim 31 further recites that the switch is comprised of "a first serial ATA port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host units." The switch in claim 31 is further comprised of "a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit." Claim 31 further recites the switch to include "a third parallel ATA port for connection to a device." Lastly, claim 31 recites that the switch is also comprised of "an arbitration and control circuit, coupled to the first, second and third

ports, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state."

Claim 32 further defines the switch in claim 31 "wherein the switch is a serial ATA switch."

Claim 35 further defines the switch in claim 31 "wherein said third parallel ATA port includes a device task file."

Claim 36 further defines the switch in claim 31 "wherein said device is a storage unit"

Claim 37 further defines the switch in claim 31 "wherein said switch is employed in an enterprise system."

Claim 38 further defines the switch in claim 31 "wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units."

Claim 39 further defines the switch in claim 31 "wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units."

Claim 40 further defines the switch in claim 39. Thus, claim 40 recites "wherein the information is referred to as 'identity drive response.'"

Claim 41 further defines the switch in claim 39 "wherein the information is referred to as 'Tag.'"

Claim 42 further defines the switch in claim 31 "wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device."

Claim 43 further defines the switch in claim 42 "wherein the information is referred to as 'Tag.'"

Mapping of Independent Claims

The independent claims are listed below, and mapped to specifications by page and line number and to the drawings.

Claim 1

Claim 1: A switch coupled between a plurality of host units and a device for communicating therebetween and comprising:

a) a first serial advanced technology attachment (ATA) port coupled to a first host unit and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;

b) a second serial ATA port coupled to a second host unit and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;

c) a third parallel ATA port, coupled to a device, for causing access to the device, by the first or second host units; and

d) an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Subject Matter	Reference to Figs	Reference to Specs
A switch	Fig. 5 Block 200 Fig. 6 Block 300 Fig. 10a Bock 500 Fig. 10b Block 500	Page 13, line 7-line 12 Page 15, lines 28-32 Page 35, lines 19-25
coupled between a plurality of host units	Fig. 5 Block 210 Fig. 5 Block 220	Page 13, line 9 Page 13, lines 16-20 Page 13, lines 26-28

and a device for communicating therebetween and comprising:	Fig. 3a item 16 Fig. 3b item 66	Page 1, lines 20 - 21
a) a first serial advanced technology attachment (ATA) port coupled to a first host unit;	Fig. 5 Block 210 Fig. 6 Blocks 310 Fig. 9 Block 410 Fig. 10a Block 510 Fig. 10b Block 510	Page 13, line 16-Page 14, line 14 Page 15, line 29-Page 16, line 3 Page 27, lines 1-5 Page 34, line 18-Page 35, line 19
and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;	Fig. 6, block labeled "Task File" inside block 310 Fig. 9, block 413a Fig. 10a, block 513a Fig. 10b, block labeled "FIS Holding Reg" inside block 510	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11-13
b) a second serial ATA port coupled to a second host unit	Fig. 5 Block 220 Fig. 6 Block 320 Fig. 9 Block 410 Fig. 10a Block 520 Fig. 10b Block 520 Fig. 11a Block 320 Fig. 11b Block 520	Page 13, line 26-Page 14, line 3 Page 15, line 30-Page 16, line 7 Page 27, lines 6-10 Page 34, line 18-Page 35, line 19

and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;	Fig. 6 Block labeled "Task File" inside Block 310	Page 17, lines 19-20 Page 45, lines 5-6 Page 45, lines 11-13
c) a third parallel ATA port, coupled to a device, for causing access to the device, by the first or second host units; and	Fig. 5 Block 230 Fig. 6 Block 330 Fig. 10a Block 530 Fig. 10b Block 530	Page 14, lines 4-14 Page 16, lines 7-11 Page 37, lines 17-18
an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.	Fig. 10a(ii) Fig. 10b(ii) Fig. 11a(ii) Fig. 11b(i)	Page 16, lines 17-20 Page 16, line 25-Page 17, line 4 Page 17, line 18-Page 18, line 2 Page 18, lines 17-20 Page 24, lines 1-5 Page 24, lines 7-12 Page 26, lines 22-23 Page 37, line 25-Page 38, line 9 Page 38, lines 18-20 Page 38, lines 21-25 Page 38, lines 27-31 Page 39, lines 2-7

Claim 18

Claim 18: A switch comprising:

a. a first serial advanced technology attachment (ATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

b. a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

c. a third parallel ATA port for connection to a device; and

an arbitration and control circuit, coupled to the first, second and third ports, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Subject Matter	Reference to Figs	Reference to Specs
A switch comprising:	Fig. 5 Block 200 Fig. 6 Block 300 Fig. 10a Bock 500 Fig. 10b Block 500	Page 13, line 7-line 12 Page 15, lines 28-32 Page 35, lines 19-25
a first serial advanced technology attachment (ATA) port for connection to a first host unit,	Fig. 5 Block 210 Fig. 6 Blocks 310 Fig. 9 Block 410 Fig. 10a Block 510 Fig. 10b Block 510	Page 13, line 16-Page 14, line 14 Page 15, line 29-Page 16, line 3 Page 27, lines 1-5 Page 34, line 18-Page 35, line 19

the first port including a first host task file responsive to commands sent by the first host unit;	Fig. 6, block labeled "Task File" inside block 310 Fig. 9, block 413a Fig. 10a, block 513a Fig. 10b, block labeled "FIS Holding Reg" inside block 510	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11-13
b) a second serial ATA port for connection to a second host unit,	Fig. 5 Block 220 Fig. 6 Block 320 Fig. 9 Block 410 Fig. 10a Block 520 Fig. 10b Block 520 Fig. 11a Block 320 Fig. 11b Block 520	Page 13, line 26-Page 14, line 3 Page 15, line 30-Page 16, line 7 Page 27, lines 6-10 Page 34, line 18-Page 35, line 19
the second port including a second host task file responsive to commands sent by the second host unit;	Fig. 6, block labeled "Task File" inside block 320 Fig. 9, block 413a Fig. 10a, block 523a Fig. 10b, block labeled "FIS Holding Reg" inside block 520	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11-13
c) a third parallel ATA port for connection to a device;	Fig. 5 Block 230 Fig. 6 Block 330 Fig. 10a Block 530 Fig. 10b Block 530	Page 14, lines 4-14 Page 16, lines 7-11 Page 37, lines 17-18

and an arbitration and control circuit, coupled to the first, second and third ports, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.	Fig. 10a(ii) Fig. 10b(ii) Fig. 11a(ii) Fig. 11b(i)	Page 16, lines 17-20 Page 16, line 25-Page 17, line 4 Page 17, line 18-Page 18, line 2 Page 18, lines 17-20 Page 24, lines 1-5 Page 24, lines 7-12 Page 26, lines 22-23 Page 37, line 25-Page 38, line 9 Page 38, lines 18-20 Page 38, lines 21-25 Page 38, lines 27-31 Page 39, lines 2-7

Claim 31

Claim 31: A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, said switch comprising:

a. a first serial ATA port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

b. a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

c. a third parallel ATA port for connection to a device; and

d. an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Subject Matter	Reference to Figs	Reference to Specs
A switch	Fig. 5 Block 200 Fig. 6 Block 300 Fig. 10a Bock 500 Fig. 10b Block 500	Page 13, line 7-line 12 Page 15, lines 28-32 Page 35, lines 19-25
that is connectable to a first host unit,	Fig. 3a item 11 Fig. 3b item 11	
a second host unit	Fig. 3a item 12 Fig. 3b item 12	
and a device	Fig. 3a item 16	Page 1, lines 20 - 21
via serial advanced technology attachment (ATA) links, said switch comprising:	Fig. 5, items 211rx 211tx, 231rx, 231tx, 221rd, 221tx Fig. 6, items 311rx, 311tx, 321rx, 321tx,	Page 13, lines 17 – 18, 26 - 29 Page 14, lines 5- 7 Page 15, line 32 – page

	331rx, 331tx Fig. 9 items 411rx, 411tx Fig. 10a items 511tx, 511rx, 521tx, 521rx, 531tx, 531rx Fig. 10b items 511tx, 511rx, 521tx, 521rx, 531tx, 531rx	16 line 9 Page 36, lines 1-2, 9-10, 17 – 18 Page 37, lines 1 - 2, 9-10, 17 - 18
a. a first serial ATA port	Fig. 5 Block 210 Fig. 6 Blocks 310 Fig. 9 Block 410 Fig. 10a Block 510 Fig. 10b Block 510	Page 13, line 16-Page 14, line 14 Page 15, line 29-Page 16, line 3 Page 27, lines 1-5 Page 34, line 18-Page 35, line 19
for connection of a first host unit,	Fig. 3a item 11 Fig. 3b item 11	
the first port including a first host task file responsive to commands sent by the first host unit;	Fig. 6, block labeled "Task File" inside block 310 Fig. 9, block 413a Fig. 10a, block 513a Fig. 10b, block labeled "FIS Holding Reg" inside block 510	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11-13
b. a second serial ATA port	Fig. 5 Block 220 Fig. 6 Block 320	Page 13, line 26-Page 14, line 3

	Fig. 9 Block 410 Fig. 10a Block 520 Fig. 10b Block 520 Fig. 11a Block 320 Fig. 11b Block 520	Page 15, line 30-Page 16, line 7 Page 27, lines 6-10 Page 34, line 18-Page 35, line 19
for connection to a second host unit,	Fig. 3a item 12 Fig. 3b item 12	
the second port including a second host task file responsive to commands sent by the second host unit;	Fig. 6 Block labeled "Task File" inside Block 310	Page 17, lines 19-20 Page 45, lines 5-6 Page 45, lines 11-13
c. a third parallel ATA port for connection to a device; and	Fig. 5 Block 230 Fig. 6 Block 330 Fig. 10a Block 530 Fig. 10b Block 530	Page 14, lines 4-14 Page 16, lines 7-11 Page 37, lines 17-18
d. an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.	Fig. 10a(ii) Fig. 10b(ii) Fig. 11a(ii) Fig. 11b(i)	Page 16, lines 17-20 Page 16, line 25-Page 17, line 4 Page 17, line 18-Page 18, line 2 Page 18, lines 17-20 Page 24, lines 1-5 Page 24, lines 7-12 Page 26, lines 22-23 Page 37, line 25-Page 38, line 9 Page 38, lines 18-20

		Page 38, lines 21-25 Page 38, lines 27-31 Page 39, lines 2-7

VIII. LISTING OF CLAIMS

Claim 1: A switch coupled between a plurality of host units and a device for communicating therebetween and comprising:

a) a first serial advanced technology attachment (ATA) port coupled to a first host unit and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;

b) a second serial ATA port coupled to a second host unit and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;

a third parallel ATA port, coupled to a device, for causing access to the device, by the first or second host units; and

an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Claim 4: A switch as recited in claim 1 wherein said third parallel ATA port includes a device task file.

Claim 5: A switch as recited in claim 4 wherein said first, second and third ports are level 4 ports.

Claim 6: A switch as recited in claim 1 wherein said device is a storage unit.

Claim 7: A switch as recited in claim 1 wherein said switch is employed in an enterprise system.

Claim 8: A switch as recited in claim 1 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 9: A switch as recited in claim 1 wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units.

Claim 10: A switch as recited in claim 9 wherein the information is referred to as 'identity drive response'.

Claim 11: A switch as recited in claim 9 wherein the information is referred to as 'Tag.

Claim 12: A switch as recited in claim 1 wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device.

Claim 13: A switch as recited in claim 12 wherein the information is referred to as 'Tag'.

Claim 14: A switch as recited in claim 13 wherein the arbitration and control circuit include a Tag/Sactive Mapping Circuit for mapping a host tag to a device tag and inverse mapping for identifying a host.

Claim 15: A switch as recited in claim 1 wherein either the first or the second host sends a legacy queue command queued by the device.

Claim 16: A switch as recited in claim 1 wherein either the first or the second host sends a native queue command for execution thereof by the device.

Claim 17: A switch as recited in claim 1 wherein the first, second and third ports are level 3 ports and a Data frame information system (FIS) first-in-first-out (FIFO) and an associated FIFO Control are coupled to the first, second and third ports and located external thereto.

Claim 18: A switch comprising:

a first serial advanced technology attachment (ATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA port for connection to a device; and

an arbitration and control circuit, coupled to the first, second and third ports, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Claim 19: A switch as recited in claim 18 wherein the switch is a serial ATA switch.

Claim 22: A switch as recited in claim 18 wherein said third parallel ATA port includes a device task file.

Claim 23: A switch as recited in claim 18 wherein said device is a storage unit.

Claim 24: A switch as recited in claim 18 wherein said switch is employed in an enterprise system.

Claim 25: A switch as recited in claim 18 wherein said arbitration circuit causes concurrent access of the device by the first and second host units.

Claim 26: A switch as recited in claim 18 wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units.

Claim 27: A switch as recited in claim 26 wherein the information is referred to as 'identity drive response'.

Claim 28: A switch as recited in claim 26 wherein the information is referred to as 'Tag".

Claim 29: A switch as recited in claim 18 wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device.

Claim 30: A switch as recited in claim 28 wherein the information is referred to as 'Tag'.

Claim 31: A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, said switch comprising:

a first serial ATA port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA port for connection to a device; and

d. an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Claim 32: A switch as recited in claim 31 wherein the switch is a serial ATA switch.

Claim 35: A switch as recited in claim [[34]] 31 wherein said third parallel ATA port includes a device task file.

Claim 36: A switch as recited in claim 31 wherein said device is a storage unit.

Claim 37: A switch as recited in claim 31 wherein said switch is employed in an enterprise system.

Claim 38: A switch as recited in claim 31 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 39: A switch as recited in claim 31 wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units.

Claim 40: A switch as recited in claim 39 wherein the information is referred to as 'identity drive response'.

Claim 41: A switch as recited in claim 39 wherein the information is referred to as 'Tag'.

Claim 42: A switch as recited in claim 31 wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device.

Claim 43: A switch as recited in claim 42 wherein the information is referred to as 'Tag'.

IX. APPENDIX

A. EVIDENCE APPENDIX: None

B. RELATED PROCEEDINGS APPENDIX: None